

***HSIM-VCS-SystemVerilog  
Verification Flow for Image Sensor  
innovative chip design***

Vladimir Polyak

Sense of **Enlightenment**

# Advasense overview

## Fabless CMOS Image Sensor startup

- Funded Q4/04
- 35 employees

## Value proposition :

- On Chip Integrated Still Image Stabilization – Virtual Tripod
- Outstanding image quality in all lighting conditions
- High Performing Small Pixel

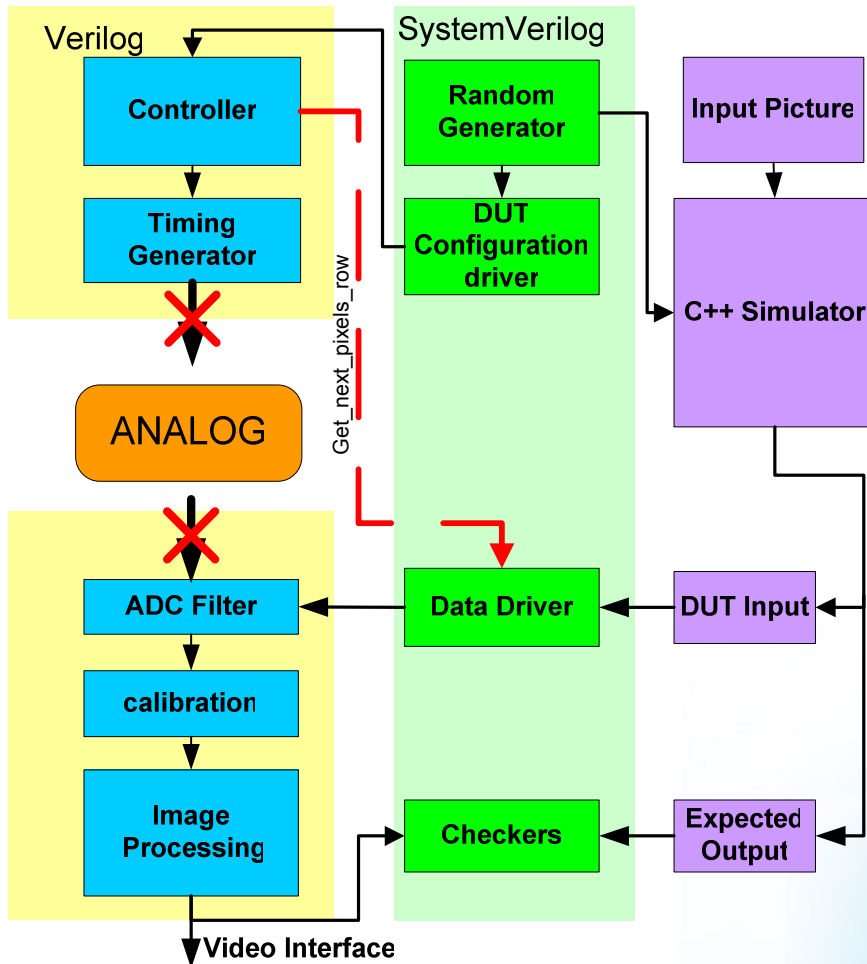
- A3000 project
- Initial verification approach
- Full chip co-simulation
- Conclusion

- A3000 is an innovative CMOS Image Sensor. CIS design for small form factor cameras requires :
  - Ridiculously small leakage, measured in few electrons per pixel → Playing with many subtle voltages to control the pixel
  - Perfect Readout → Very small temporal noise → innovative feedback design that requires very tight digital control
  - Excellent ADC : 14-bit @ 80Mhz, implemented as a complex column parallel analog+digital 1024 ADCs
  - extremely small pixel → complex transistor sharing structure
- Advasense unique Image Stabilization on chip adds challenges :
  - Pixel that is writable → Complex feedback & store
  - Digital signal processing to identify camera motion and compensate

- CIS sensor design is the art of making a whole array of pixels fully calibrated and with low visible noise with the highest accuracy of details.
  - Noise sources are numerous : electrical, optic, non-uniformities
  - The CIS behavior with all the noises is modeled by a C++/Matlab model
  - The simulation results are used to build analog & digital compensation & calibration mechanisms
  - Image Stabilization at low light doubles the effort to compensate & calibrate.

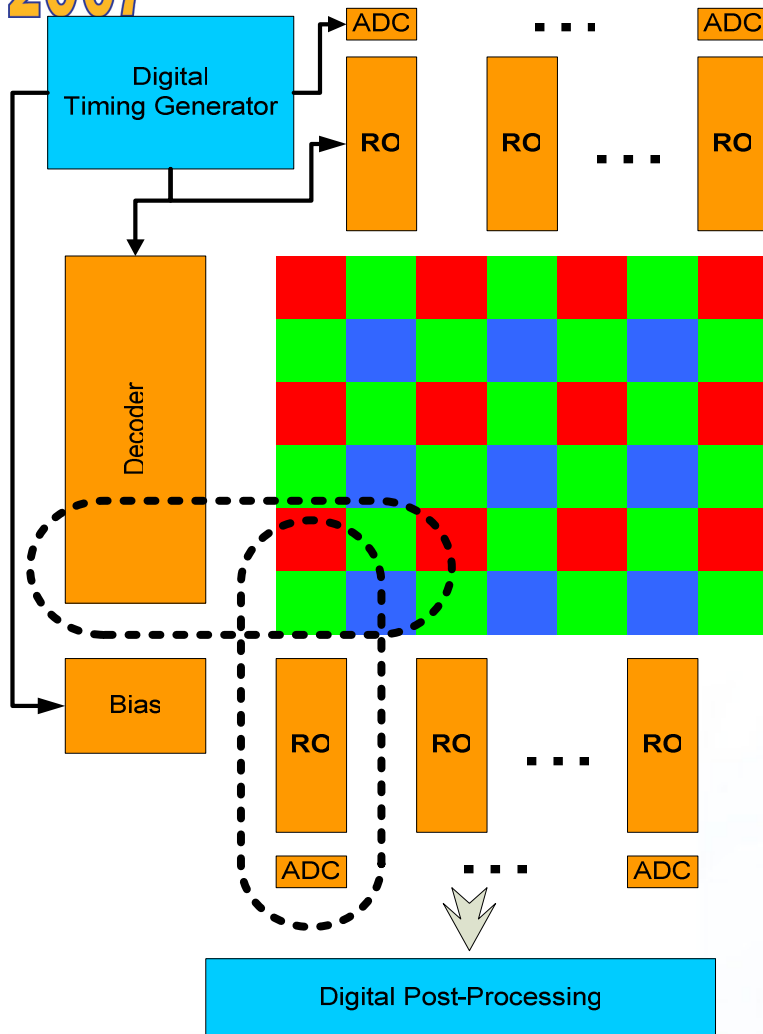
# A3000 block diagram

- A3000 is combined of an analog & digital blocks:
- Analog :
  - Pixel array + decoder
  - ReadOut
  - Bias generators
  - Column parallel ADC - mix signal
- Digital :
  - Host interface
  - Controller & timing generator
  - Calibration
  - Image processing
  - Video Interface – Parallel & Serial



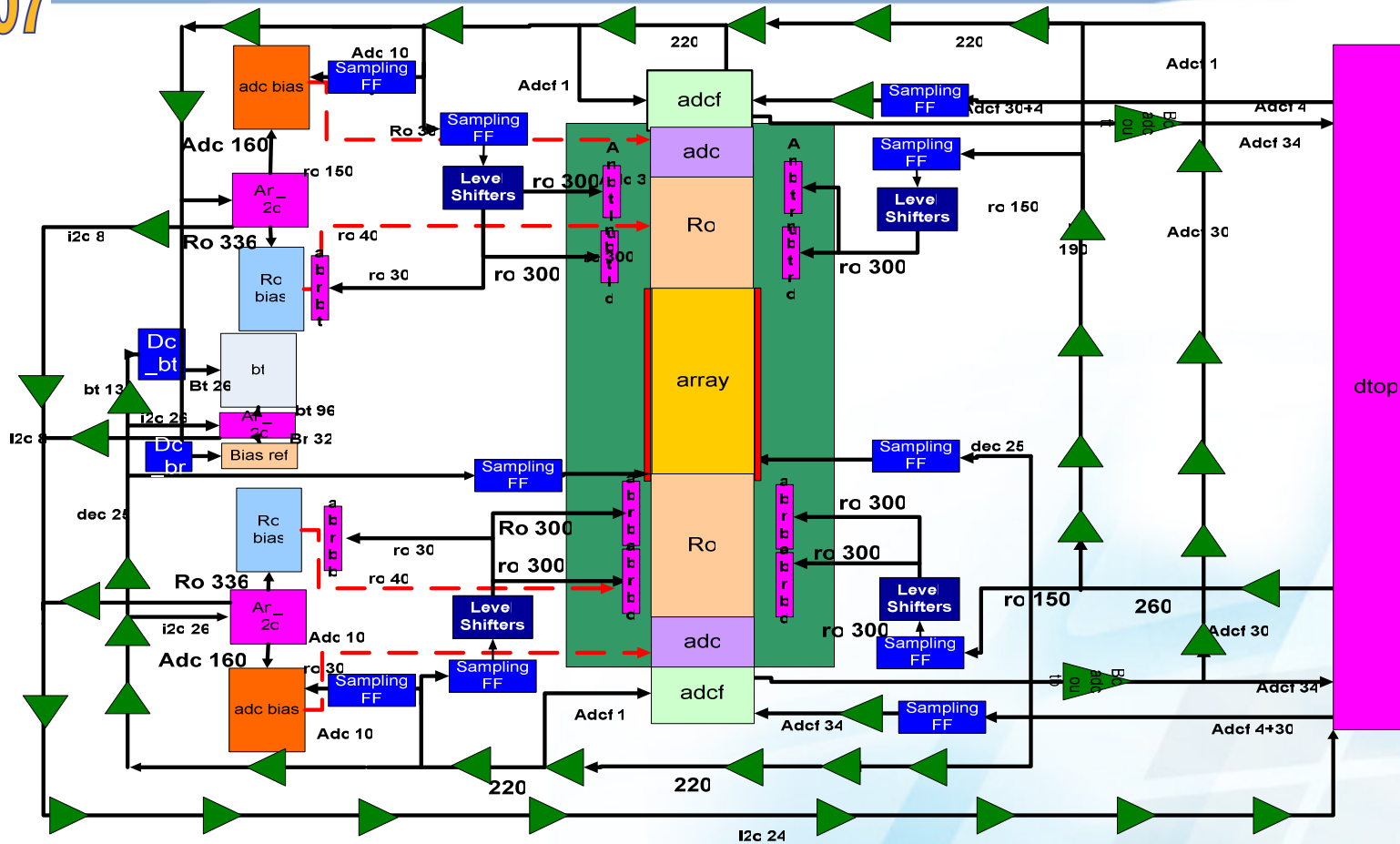
- Digital verification environment includes:
  - C++ simulator for off-line inputs and expected outputs generation.
  - SystemVerilog environment for each block; ~10 per chip.
  - "Full digital" environment that reuses block level environments based on VMM methodology.
- **Analog blocks not modeled in digital environment => Digital blocks connected to analog not fully verified.**

# Initial Verification Approach



- **Analog verification** of ARRAY/RO/ADC/Bias based on spice simulator only.
- Only one block of each type is simulated due to performance issues.
- Inter-block functionality checked on reduced schematics.
- Digital input provided in PWL format.
- Simulation results evaluation based on waveforms analysis.

# A3000 top level connectivity



- Thousands nets on top level that should be verified.

# Initial approach drawbacks

- Digital blocks connected to analog not fully verified.
- Connectivity between analog and digital blocks not verified.
- Feedback loops not checked( could not be simulated using PWL vectors generated off-line ).
- Complex connectivity between analog blocks not checked.
- Analog test benches not derived from top-level schematic.
- Analog stimuli based on synthetic PWL.

We decided to address these issues in the new environment.

## Why co-simulation?

- Traditional verification approaches don't work:
  - Complex analog designs can't be modeled by RTL or verilogA.
  - Full chip can't be simulated on transistor level.
- Feedback loops can't be verified with PWL stimulus.
- Complex analog output can't be verified by visual waveform analysis. The automatic checking of data after digital post-processing is required.

## Why VCS+HSIM?

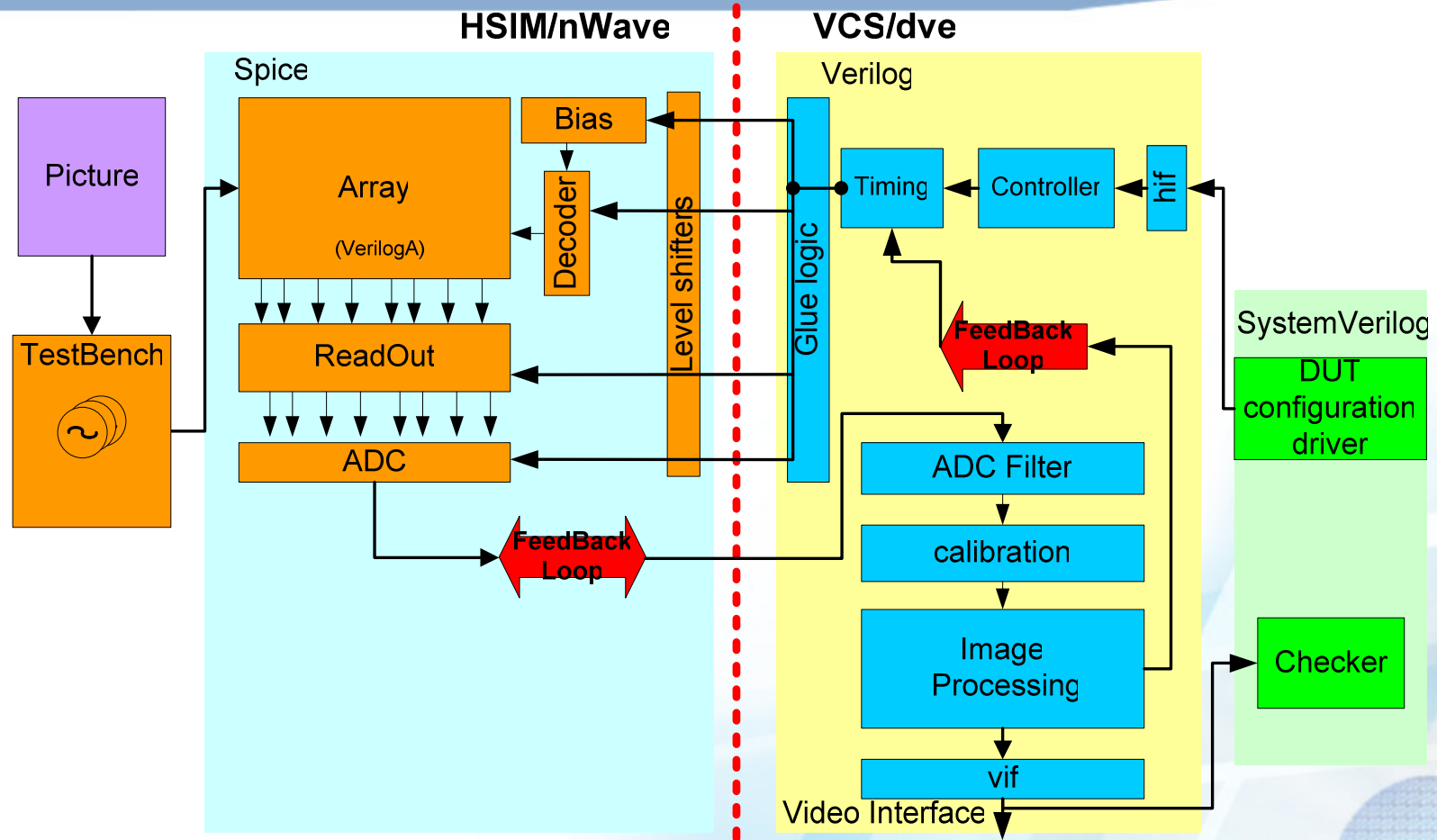
- VCS/HSIM co-simulation supports SystemVerilog  
=> Reuse of existing verification environment.
- We used HSIM for memory verification and were satisfied with results.
- Co-simulation supports behavioral modeling in VerilogA.

## Why VCS+HSIM?

Initial evaluation shown:

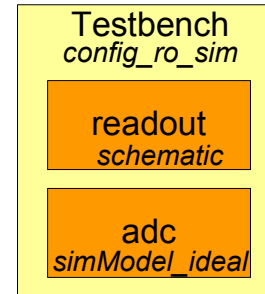
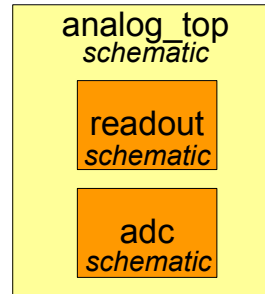
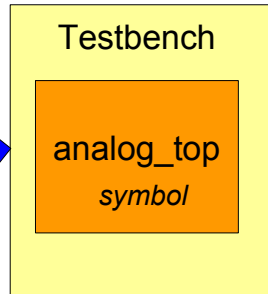
- Spice accuracy even on pixel circuitry – very sensitive and uncommon circuit with low current resolution.
- **HSIM Isomorphic Matching** that eliminates redundant computation on identical blocks provides enormous runtime improvement. Runtime of 1000 ADC only twice larger than the runtime of single ADC.
- Capacity was checked by simulating 1000 ADCs.
- Fast Ramp-up. In several days real co-simulation test was up and running.

# Full chip verification environment



- Verification driven design partitioning is crucial.

Script converts symbol to verilog envelope with extended busses. Instantiation in the top verilog also produced.



Spice netlist created from config view.

```

module analog_top( gt_dec_sel_0, gt_dec_sel_1, gt_dec_sel_2, gt_dec_rst, .. );
  input gt_dec_sel_0, gt_dec_sel_1, gt_dec_sel_2 ;
  input gt_dec_rst ;
  .....
`ifdef COSIM
  initial $nsda_module();
`endif
endmodule

module a3000_top();
  wire gt_dec_sel[3];
  wire gt_dec_rst ;
  analog_top analog_top( .gt_dec_sel_0(gt_dec_sel[0]), .gt_dec_sel_1(gt_dec_sel[1]),
    .gt_dec_sel_2(gt_dec_sel[2]), .gt_dec_rst(gt_dec_rst), ... );
endmodule
  
```

```

.SUBCKT ANALOG_TOP
+ gt_dec_sel_0 gt_dec_sel_1
+ gt_dec_sel_2 gt_dec_rst
.....
.ENDS
  
```

- Simulation netlist always derived from real top-level schematic and top-level verilog.

## Runtime – is crucial

- Simulating all analog blocks at transistor level is still time consuming and should be done during final sign-off. On debugging stages we used heuristics:
  - Blocks that not under test represented by empty, ideal or verilogA schematics.
  - System clock inside analog logic forced to 0, when logic functionality is not important (using `.force` and `.release` HSIM commands)
  - Initial conditions set on Bias nodes to reduce convergence time (using `.ic`).
  - VerilogA model of ADC was developed (VerilogA for pixel doesn't work.)
- Determine HSIM parameters for each analog block according to accuracy vs performance tradeoff.

# Trimming signals verification

There are ~400 trimming signals between analog and digital that could not be verified functionally as their influence is not obvious. Correspondence between digital and analog names stored in excel table.

## We developed VerilogA testbench for these signals:

- Each analog block was replaced by VerilogA that monitors trimming values and reports their change.
- All trimming values were changed one by one by SystemVerilog driver according to the table order.
- Script checked order of the signals reported by verilogA according to excel table.

# Conclusions

- VCS/SystemVerilog/HSIM co-simulation provides many benefits:
  - Verification of feedback loops.
  - Building regression tests environment for analog blocks.
  - “Big A, Big D” full chip verification.
- VerilogA is not well supported in HSIM.
- **VCS/SystemVerilog/HSIM co-simulation is ready for real work and fast ramp-up.**

# Acknowledgements

- Co-Author
  - Itzik Zafrany, Synopsys